Bo-Wen Chen

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Education

National Taiwan University (NTU) — Taipei, Taiwan

M.S. in Graduate Institute of Communication Engineering (Advisor: Hung-yi Lee) — Sep. 2018 - Nov. 2022

- Selected Courses: Introduction to Digital Speech Processing, Deep Learning for Computer Vision, Data Science

National Taiwan University (NTU) — Taipei, Taiwan

B.S. in Electrical Engineering (Overall GPA: 3.5/4.3, Last 60: 3.8/4.3) — Sep. 2014 - Jun. 2018

- Selected Courses: Machine Learning, Mathematical Principles for Machine Learning, Advanced Digital Signal Processing, Convex Optimization, Computer Architecture, Introduction to Electronic Design Automation, Algorithms, Data Structure and Programming

Skills

Core competencies	Machine Learning, Digital Speech Processing, UNIX-like Operating Systems
Languages	Python, C/C++, Shell Scripting, Verilog, LaTeX
Libraries & Platforms	Fairseq, NeMo, PyTorch, Pytorch Lightning, TensorFlow, Kaldi, Git, Arch Linux

Research Experience

Speech Processing & Machine Learning Laboratory, NTU — Taipei, Taiwan

Graduate Researcher, supervised by Prof. Hung-Yi Lee — Sep. 2018 - Nov. 2022

- Conducted research in speech processing and acoustic modeling utilizing deep learning techniques to explore novel topics
- Developed **first duplex speech chain model** for concurrent Text-to-Speech (TTS) and Automatic Speech Recognition (ASR) via a single reversible network, delivering decent performance with metrics like 4.116 MCD for TTS and 27.96 PER for ASR [1]
- Proposed an efficient neural architecture search technique for audio source separation, reducing search time by 50% by leveraging on the signal to distortion ratio (SDR) correlation between randomly weighted and fully trained models [2]
- Served as a reviewer for ICASSP 2020

Network Administrator — Sep. 2018 - Jun. 2020

- Managed a large-scale cluster infrastructure based on Slurm (10 nodes, over 20 GPUs), and addressed issues for more than 30 users
- Implemented maintenance scripts for rapid system upgrade on all Arch Linux nodes within the cluster

Publications

[1] **Bo-Wen Chen**, **An Analysis of Duplex Sequence-to-Sequence Learning for Speech Chain**, Master's thesis, National Taiwan University Theses and Dissertations Repository, 2022. [link]

[2] **Bo-Wen Chen**, Yen-Min Hsu, and Hung-Yi Lee, **J-Net: Randomly Weighted U-Net for Audio Source Separation**, CoRR, abs/1911.12926 (arXiv preprint), 2019. [link][Github]

Work Experience

WinYam Innovative Studio — Taipei, Taiwan

Co-Founder & CTO, self-employed — Sep. 2015 - Nov. 2022

- Oversaw the development, testing, and launch of new features/modules for a WebRTC-based tour guide system [link]
- Provided a LAN-based solution with a portable device and a pay-per-use cloud service, serving 1000+ users

Acoustic and Speech Processing Team of Multimedia Department, MediaTek — Hsinchu, Taiwan

Software Engineer Intern, supervised by Yiou-Wen Cheng — Jul. 2017 - Aug. 2017

- Compressed acoustic models for compute-constrained embedded systems via SVD, sustaining performance with 50% fewer parameters
- Created a toolkit to facilitate seamless migration of acoustic models from Kaldi to Tensorflow, effectively reducing development time

Institute of Information Science, Academia Sinica — Taipei, Taiwan

Research Assistant, supervised by Dr. Tyng-Luh Liu — Jul. 2016 - Aug. 2016

- Reimplemented a super-resolution model, which predicted the residual between the original image and its super-resolved counterpart

Awards and Projects

Honorable Mention Award — Ministry of Education, Taiwan

AI CUP - Abstract Label Classification Competition [link] — Built with Pytorch and Fairseq

- Achieved 8th place out of 469 teams as team leader, with a micro-F1 score of 0.721 on the leaderboard
- Used pretrained language models, SCIBERT, with additional linear layers to perform sequential sentence classification [Github]

5-stage pipelined MIPS processor — National Taiwan University, Taiwan

Computer Architecture, EE 4039 — Built with Verilog

- Optimized a RTL design of 5-stage pipelined MIPS processor in Verilog, incorporating techniques like hazard handling, branch prediction, and multi-level caching. Achieved over 10% performance improvement in cycle count
- Enhanced performance via L2 cache, optimized L1 cache with 2-way set associative, and investigated cache configurations' impacts [link]

Input Sequence Generator for System Verilog Assertion Checking — National Taiwan University, Taiwan

Introduction to Electronic Design Automation, EE 3012 — Built with C++

- Revamped assertion checking as graph reachability, achieving max failed assertions in alpha benchmark, matching 1st place team's results
- Converted System Verilog Mealy machines to Moore machines, simplifying verification by state-based output determination [link]